MP310D

S-band Phase Shifter 2.5…4 GHz

- frequency range 2.5…4 GHz
- Insertion loss 7 dB at 3 GHz
- phase shift range 355° (6 bit, 64 states, 5,625° step)

Application

- communications
- radars

The MP310D is a high performance GaAs MMIC 6-bit digital phase shifter which covers a frequency range from 2.5 to 4 GHz and can be used in telecommunication and radar applications. The on-chip digital control logic allows for parallel data input. This chip is manufactured using 0.5 µm gate length pHEMT process. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

Electrical specification (T = 25 °C)

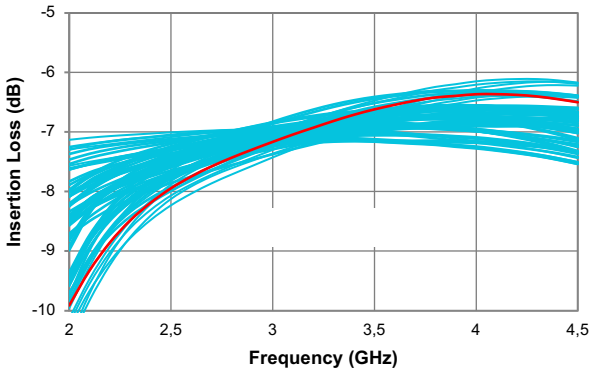
Symbol	Parameter	Min.	Typ.	Max.	Unit
ΔF	Frequency range	2.5	—	4	GHz
S21	Insertion loss	—	—	8.2	dB
S21_Var	Insertion loss variation	—	—	1.2	dB
S11	Input return loss	13	—	—	dB
S22	Output return loss	13	—	—	dB
P1dB	Input power for 1 dB compression	20	—	—	dBm
Δ_PhS	Phase shifter range	—	355	—	deg
RMS_PhS	RMS phase error	—	—	3	deg
RMS_S21	RMS amplitude error	—	—	0.3	dB
t_{rise}, t_{fall}	Switching characteristics	—	—	60	ns
VSS	Supply voltage for digital control logic	—	−5.0	—	V
VLH	Control voltage high	+2.2	+3.3	+5	V
VLL	Control voltage low	0	—	+0.7	V
I_VSS	DC current for digital control	—	—	5	mA

Absolute maximum ratings

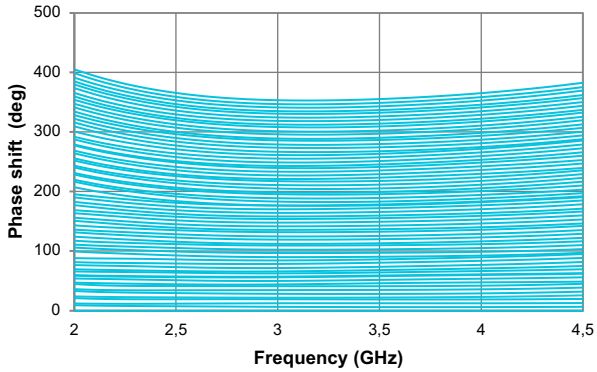
Parameter	Value	Unit
Supply voltage for digital control	−6…−4	V
Control voltages	0…+5,5	V
Operating temperature	−60…+85	°C
Storage temperature	−60…+125	°C

Typical characteristics (T = 25 °C)

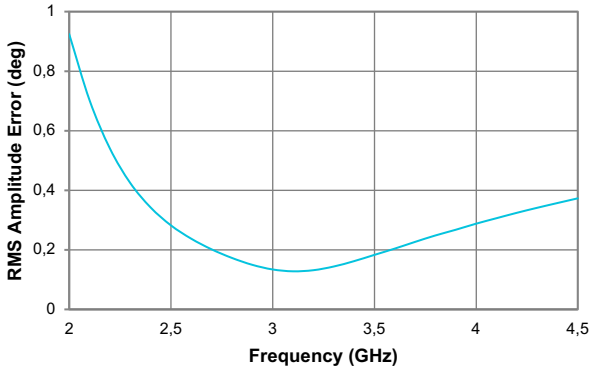
Insertion Loss



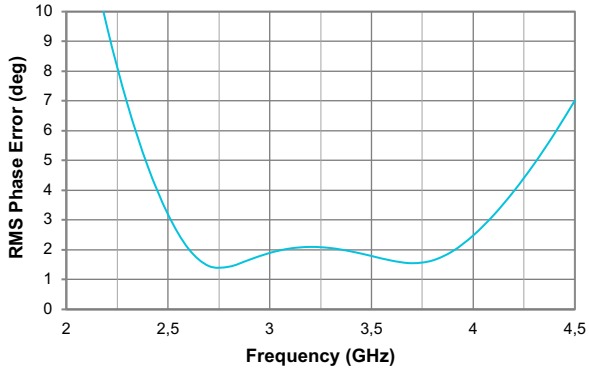
Phase shift



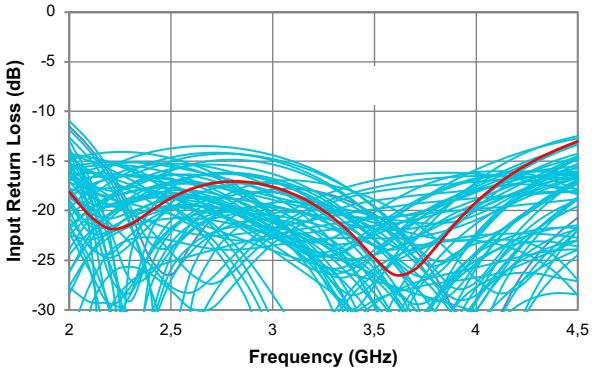
RMS Amplitude Error



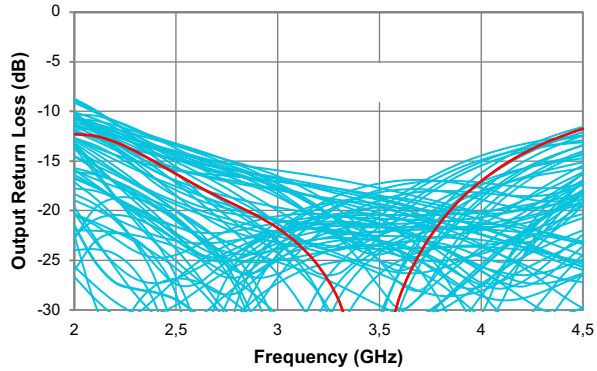
RMS Phase Error



Input Return Loss

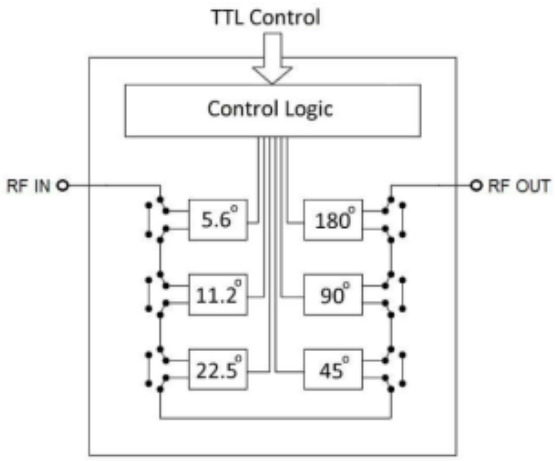


Output Return Loss



REMARK Input power level for characterization is −5 dBm.

Functional diagram

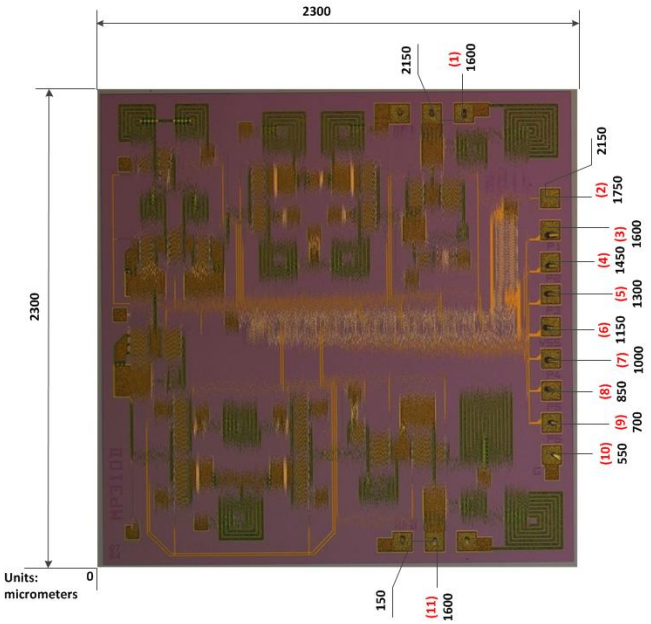


Control table

State number	Phase shift, °	Voltage to apply on the control pads					
		P6	P5	P4	P3	P2	P1
0 (REF)	0,000	0	0	0	0	0	0
1	5,625	0	0	0	0	0	1
2	11,250	0	0	0	0	1	0
4	22,500	0	0	0	1	0	0
8	45,000	0	0	1	0	0	0
16	90,000	0	1	0	0	0	0
32	180,000	1	0	0	0	0	0
63	354,375	1	1	1	1	1	1

REMARK «0» is control voltage low and, «1» is control voltage high.

Mechanical data



- Chip size 2300 × 2300 µm (before wafer dicing), thickness 100 µm;
- Bond pad dimensions are shown in the bond pad center;
- Bond pad and backside metallization: gold;
- RF pads are 100 × 100 µm.

Pad number	Port	Voltage, V	Description
1	RF IN	—	RF in port
2	—	—	Monitor of the output voltage of the control logic[1]
3	P1	0 / +3.3	Control of 5.625° phase shifter bit
4	P2	0 / +3.3	Control of 11.25° phase shifter bit
5	P3	0 / +3.3	Control of 22.5° phase shifter bit
6	VSS	−5	Supply of digital control logic
7	P4	0 / +3.3	Control of 45° phase shifter bit
8	P5	0 / +3.3	Control of 90° phase shifter bit
9	P6	0 / +3.3	Control of 180° phase shifter bit
10	GND	—	GND
11	RF OUT	—	RF out port

REMARK [1]This pad is NOT used in typical conditions.

Application notes

Mounting
The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat. The 50 Ohm Microstrip transmission lines on 0.127mm thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). One way to accomplish this is to attach the 0.102 mm thick die to a 0.150 mm thick molybdenum heat spreader (molytab) which is then attached to the ground plane (Figure 2). Microstrip substrates should be located as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.1mm.

Wire Bonding
A recommendation for RF pads (1 and 11) is one wire: diameter 25 µm, length 450 µm. A recommendation for DC and control pads (3 to 9) is one wire: diameter 25 µm, length 700- 1000 µm.

Bias Arrangement
The DC bias pad №6 needs to have DC bypass capacitance 100 pF as close to the device as possible.

Phase Shifter Control Bias
Digital control logic is integrated in the device to supply the necessary internal switching voltages for the phase shifter's cells. The reference state is enabled with logic low (0 V) on control pads of the phase shifter (3 to 5 and 7 to 9). The binary weighted phase states are switched by applying logic high on the respective control pad. A control table for the phase shifter is presented higher.

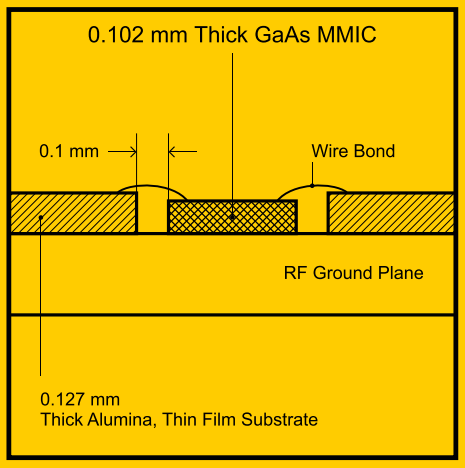


Figure 1.

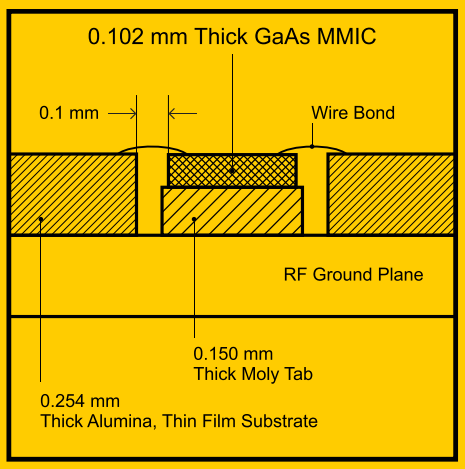


Figure 2.

Recommended ESD Management

This device is susceptible to electrostatic and mechanical damage. Dies are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded antistatic workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.