MP109D

6-bit digital attenuator 0.1…14 GHz

- frequency range 0.1 to 14 GHz
- insertion loss 5 dB at 10 GHz
- attenuation range 31.5 dB (6 bit, 64 states, 0.5 dB step)
- parallel data Input

Application

- radars
- communications
- test and measurement equipment

The MP109D is a high performance GaAs MMIC 6-bit digital attenuator which covers a frequency range from 0.1 to 14 GHz and can be used in communications, T&Ms and radars. The on-chip digital control logic is used for parallel data input. This chip is manufactured based on 0.5 µm gate length pHEMT process. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation obtaining the highest reliability level.

Electrical specification (T = 25 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
ΔF	Frequency range	0.1	—	14	GHz
S21	Insertion loss	—	—	5.5	dB
S11	Input return loss	10	—	—	dB
S22	Output return loss	10	—	—	dB
Δ_ATT	Attenuator range	—	31.5	—	dB
RMS_ATT	RMS amplitude error	—	—	0,35	dB
RMS_PhS	RMS phase error	—	—	4	deg
P1dB	Input power at 1 dB compression point	20	—	—	dBm
t_{rise}, t_{fall}	Switching characteristics	—	—	60	ns
VSS	Supply voltage for digital control logic	—	−5	—	V
VLH	Control voltage high	+2.2	+3.3	+5	V
VLL	Control voltage low	0	—	+0.7	V
I_VSS	DC current for digital control	—	—	5	mA

Absolute maximum ratings

Parameter	Value	Unit
Supply voltage for digital control	−7.5	V
Control voltages	0…+5.5	V
Operating temperature	−60…+85	°C
Storage temperature	−60…+125	°C

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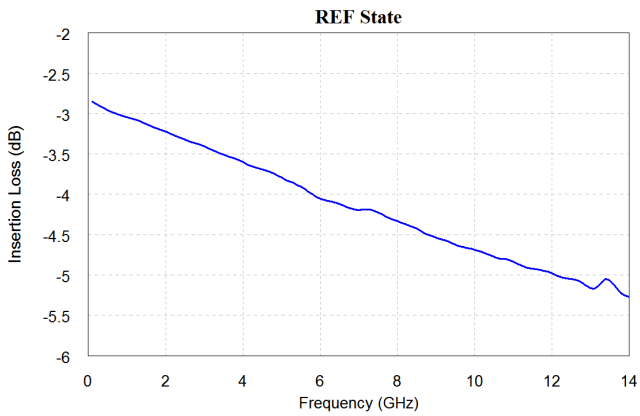
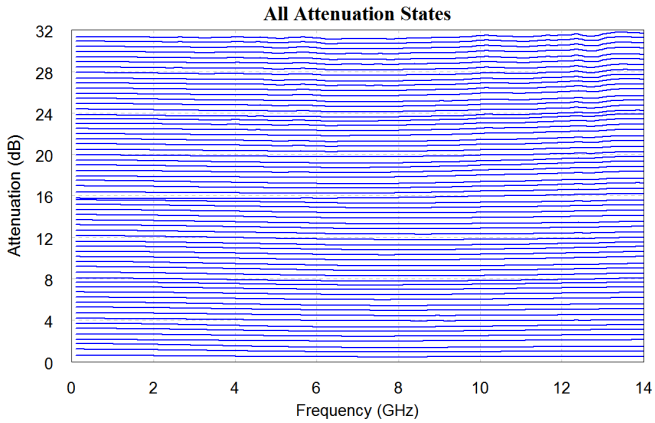
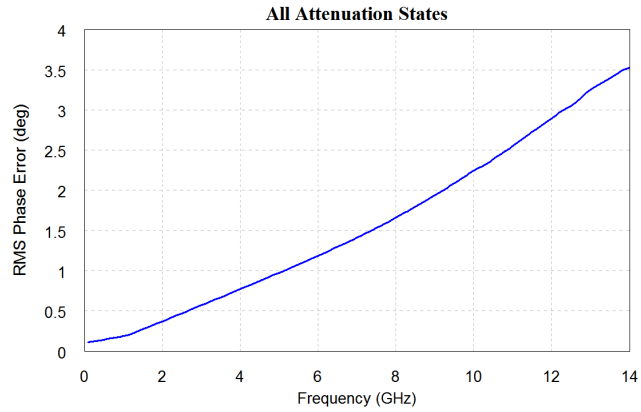
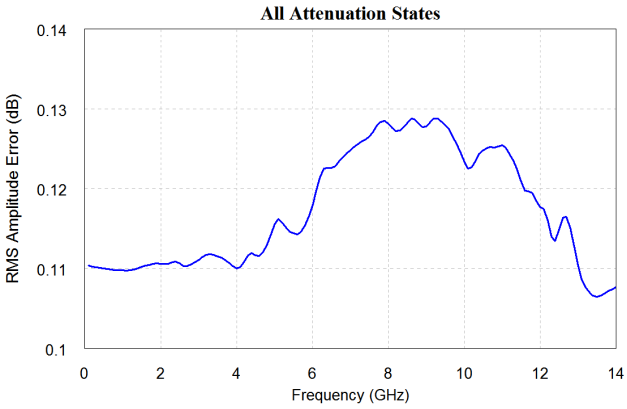
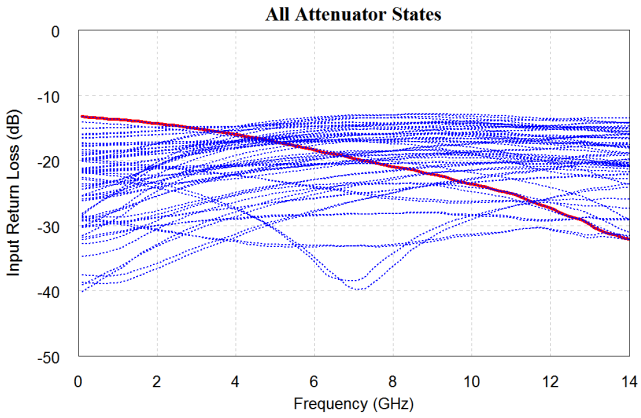
Typical characteristics (T = 25 °C)

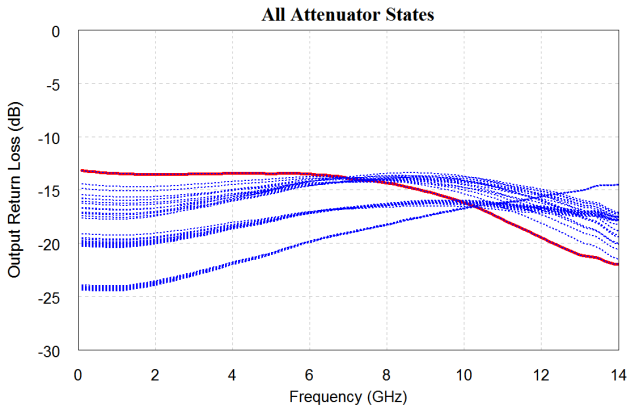






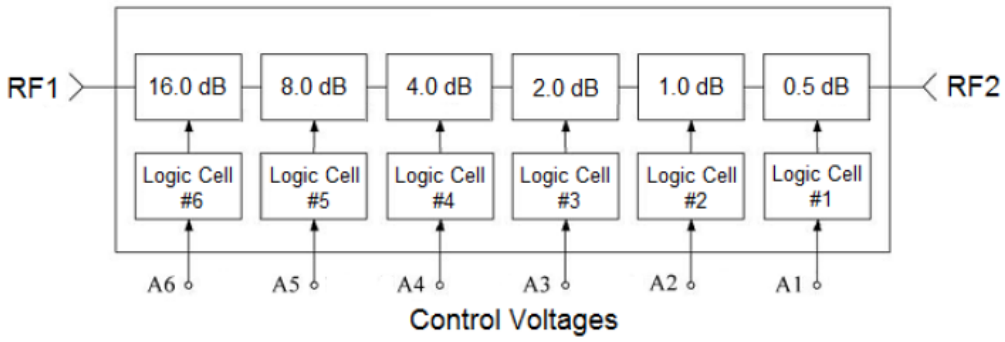






REMARK Input power level for characterization is −5 dBm.

Functional diagram

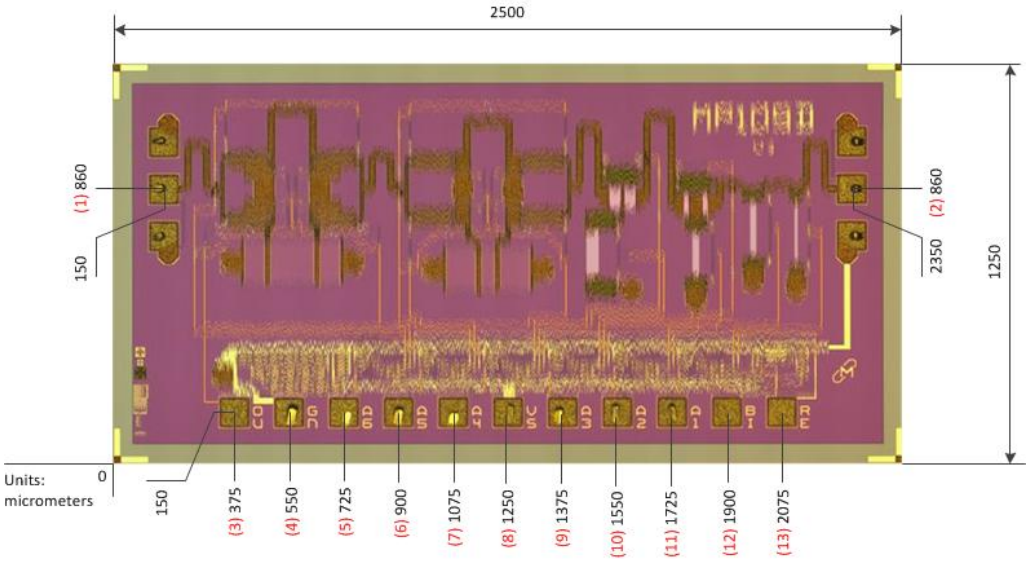


Control table

State number	Attenuation, °	Voltage to apply on the control pads					
		A6	A5	A4	A3	A2	A1
0 (REF)	0.0	0	0	0	0	0	0
1	0.5	0	0	0	0	0	1
2	1.0	0	0	0	0	1	0
4	2.0	0	0	0	1	0	0
8	4.0	0	0	1	0	0	0
16	8.0	0	1	0	0	0	0
32	16.0	1	0	0	0	0	0
63	31.5	1	1	1	1	1	1

REMARK «0» is control voltage low and, «1» is control voltage high.

Mechanical data



- Chip size 2500 × 1250 µm (before wafer dicing), thickness 100 µm;
- Bond pad dimensions are shown to centre of bond pad;
- Bond pad and backside metallization: gold;
- RF and DC pads (1 to 13) 100 ×100 µm.

Pad number	Pad ID	DC Voltage, V	Description
1	—	—	RF port 2
2	—	—	RF port 1
3	QU	—	Monitor of the output voltage of the control logic[1]
4	GN	—	Decoupling ground
5	A6	0 / +3.3	Control of 16 dB attenuator bit
6	A5	0 / +3.3	Control of 8 dB attenuator bit
7	A4	0 / +3.3	Control of 4 dB attenuator bit
8	VS	−5	Supply of digital control logic
9	A3	0 / +3.3	Control of 2 dB attenuator bit
10	A2	0 / +3.3	Control of 1 dB attenuator bit
11	A1	0 / +3.3	Control of 0.5 dB attenuator bit
12	BI	—	Reference voltage for bias generator of digital control logic[1,2]
13	RE	—	Reference voltage for digital control logic[1,2]

[1]Pad is NOT used in typical conditions
[2]Possible to use an external voltage divider in addition to integrated circuit

Application notes

Mounting
The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat. The 50 Ohm Microstrip transmission lines on 0.127mm thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). One way to accomplish this is to attach the 0.102 mm thick die to a 0.150 mm thick molybdenum heat spreader (molytab) which is then attached to the ground plane (Figure 2). Microstrip substrates should be located as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.1mm.

Wire Bonding
A recommendation for RF pads (1 and 2) is one wire: diameter 25 µm, length 450 µm. A recommendation for DC and control pads (5 to 11) is one wire: diameter 25 µm, length 700–1000 µm

Bias Arrangement
The pad №8 (VSS) needs to have DC bypass capacitance of 100 pF as close to the device as possible.

Attenuator Control Bias
Digital control logic is integrated in the device to supply the necessary internal switching voltages for the attenuator's cells. The reference state is enabled with logic low (0V) on control pads of the attenuator (5 to 7 and 9 to 11). The binary weighted attenuation states are switched by applying logic high on the respective control pad. A control table for the attenuator is presented below.

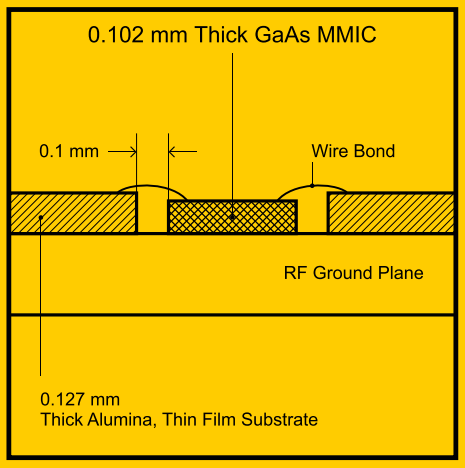


Figure 1.

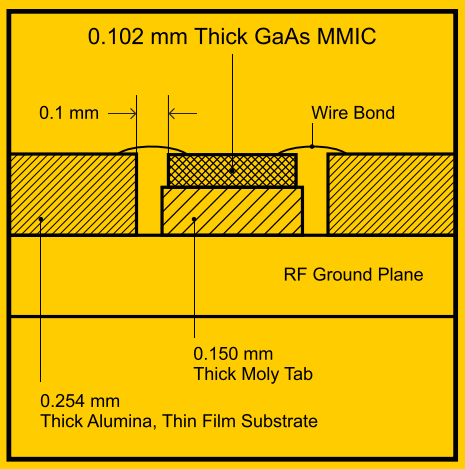


Figure 2.

Recommended ESD Management

This device is susceptible to electrostatic and mechanical damage. Dies are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded antistatic workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.